

128K x 24 Bit Static Random Access Memory

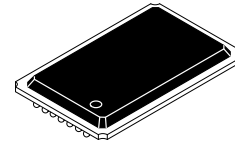
The MCM6341 is a 3,145,728-bit static random access memory organized as 131,072 words of 24 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6341 is equipped with chip enable ($\overline{E1}$, $E2$, $\overline{E3}$) and output enable (\overline{G}) pins, allowing for greater system flexibility and eliminating bus contention problems.

The MCM6341 is available in a 119-bump PBGA package.

- Single 3.3 V Power Supply
- Fast Access Time: 10/11/12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three-State Outputs
- Power Operation: 280/275/270/260 mA Maximum, Active AC
- Commercial Temperature (0°C to 70°C) and Industrial Temperature (-40°C to 85°C) Options

MCM6341

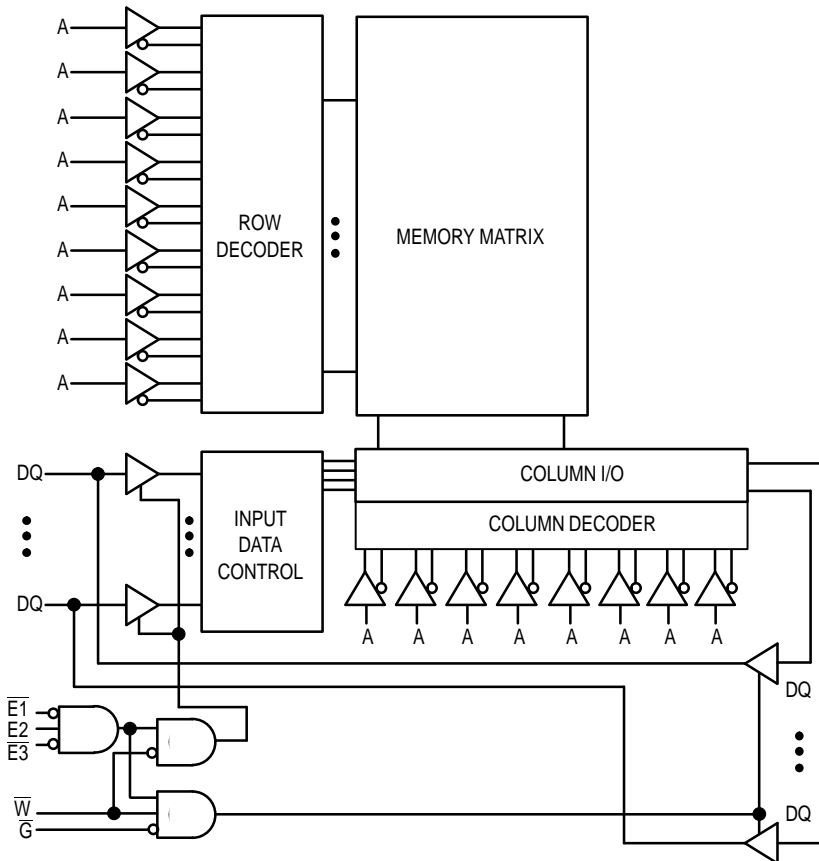


ZP PACKAGE
PBGA
CASE 999-02

PIN NAMES

A	Address Inputs
\overline{W}	Write Enable
\overline{G}	Output Enable
$\overline{E1}$, $E2$, $\overline{E3}$	Chip Enable
DQ	Data Input/Output
NC	No Connection
VDD	+ 3.3 V Power Supply
VSS	Ground

BLOCK DIAGRAM



REV 8
10/6/99

PIN ASSIGNMENT

	1	2	3	4	5	6	7
A	○ NC	○ A	○ A	○ A	○ A	○ A	○ NC
B	○ NC	○ A	○ A	○ $\overline{E1}$	○ A	○ A	○ NC
C	○ DQ	○ NC	○ E2	○ NC	○ $\overline{E3}$	○ NC	○ DQ
D	○ DQ	○ VDD	○ VSS	○ VSS	○ VSS	○ VDD	○ DQ
E	○ DQ	○ VSS	○ VDD	○ VSS	○ VDD	○ VSS	○ DQ
F	○ DQ	○ VDD	○ VSS	○ VSS	○ VSS	○ VDD	○ DQ
G	○ DQ	○ VSS	○ VDD	○ VSS	○ VDD	○ VSS	○ DQ
H	○ DQ	○ VDD	○ VSS	○ VSS	○ VSS	○ VDD	○ DQ
J	○ VDD	○ VSS	○ VDD	○ VSS	○ VDD	○ VSS	○ VDD
K	○ DQ	○ VDD	○ VSS	○ VSS	○ VSS	○ VDD	○ DQ
L	○ DQ	○ VSS	○ VDD	○ VSS	○ VDD	○ VSS	○ DQ
M	○ DQ	○ VDD	○ VSS	○ VSS	○ VSS	○ VDD	○ DQ
N	○ DQ	○ VSS	○ VDD	○ VSS	○ VDD	○ VSS	○ DQ
P	○ DQ	○ VDD	○ VSS	○ VSS	○ VSS	○ VDD	○ DQ
R	○ DQ	○ NC	○ NC	○ NC	○ NC	○ NC	○ DQ
T	○ NC	○ A	○ A	○ \overline{W}	○ A	○ A	○ NC
U	○ NC	○ A	○ A	○ \overline{G}	○ A	○ A	○ NC

**119-BUMP PBGA
TOP VIEW**

TRUTH TABLE (X = Don't Care)

$\bar{E}1$	E2	$\bar{E}3$	\bar{G}	\bar{W}	Mode	I/O Pin	Cycle	Current
H	X	X	X	X	Not Selected	High-Z	—	I _{SB1} , I _{SB2}
X	L	X	X	X	Not Selected	High-Z	—	I _{SB1} , I _{SB2}
X	X	H	X	X	Not Selected	High-Z	—	I _{SB1} , I _{SB2}
L	H	L	H	H	Output Disabled	High-Z	—	I _{DDA}
L	H	L	L	H	Read	D _{out}	Read	I _{DDA}
L	H	L	X	L	Write	High-Z	Write	I _{DDA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V _{SS}	V _{DD}	-0.5 to 5.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{DD}	V _{in} , V _{out}	-0.5 to V _{DD} + 0.5	V
Output Current (per I/O)	I _{out}	±20	mA
Power Dissipation	P _D	1.0	W
Temperature Under Bias	T _{bias}	-10 to 85	°C
Commercial Industrial		-45 to 90	
Storage Temperature — Plastic	T _{stg}	-55 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

PRODUCT CONFIGURATIONS

Part No.	Commercial	Industrial	Power Supply	
			+ 10%, - 5%	± 10%
MCM6341ZP10	✓			✓
MCM6341ZP11	✓			✓
MCM6341ZP12	✓			✓
MCM6341ZP15	✓			✓
SCM6341ZP10C		✓	✓	
SCM6341ZP11A		✓		✓
SCM6341ZP12A		✓		✓
SCM6341ZP15A		✓		✓

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{DD} = 3.3 \text{ V} \pm 10\%$, $T_A = 0^\circ \text{ to } 70^\circ \text{C}$)
 ($T_A = -40^\circ \text{ to } 85^\circ \text{C}$ for Industrial Temperature Option)
 ($V_{DD} = 3.3 \text{ V} + 10\%$, -5% for 10 ns Industrial Device Only)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	$V_{DD} + 0.3^{**}$	V
Input Low Voltage	V_{IL}	-0.5^*	—	0.8	V

* $V_{IL}(\text{min}) = -0.5 \text{ V dc}$; $V_{IL}(\text{min}) = -2.0 \text{ V ac}$ (pulse width $\leq 2.0 \text{ ns}$).

** $V_{IH}(\text{max}) = V_{DD} + 0.3 \text{ V dc}$; $V_{IH}(\text{max}) = V_{DD} + 2.0 \text{ V ac}$ (pulse width $\leq 2.0 \text{ ns}$).

DC CHARACTERISTICS (See Note)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0 \text{ to } V_{DD}$)	$I_{lkg}(I)$	—	± 1.0	μA
Output Leakage Current ($\bar{E} = V_{IH}$, $V_{out} = 0 \text{ to } V_{DD}$)	$I_{lkg}(O)$	—	± 1.0	μA
Output Low Voltage ($I_{OL} = +8.0 \text{ mA}$)	V_{OL}	—	0.4	V
Output High Voltage ($I_{OH} = -4.0 \text{ mA}$)	V_{OH}	2.4	—	V

NOTE: $\bar{E}1$, $E2$, and $\bar{E}3$ are represented by \bar{E} in this data sheet. $E2$ is of opposite polarity to $\bar{E}1$ and $\bar{E}3$.

POWER SUPPLY CURRENTS (See Note)

Parameter	Symbol	0 to 70°C	- 40 to 85°C	Unit
AC Active Supply Current ($I_{out} = 0 \text{ mA}$, $V_{DD} = \text{max}$)	MCM6341-10 MCM6341-11 MCM6341-12 MCM6341-15 I_{DD}	250 240 230 220	290 285 280 270	mA
AC Standby Current ($V_{DD} = \text{max}$, $\bar{E} = V_{IH}$, No other restrictions on other inputs)	MCM6341-10 MCM6341-11 MCM6341-12 MCM6341-15 I_{SB1}	50 50 50 45	55 55 55 50	mA
CMOS Standby Current ($\bar{E} \geq V_{DD} - 0.2 \text{ V}$, $V_{in} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{DD} - 0.2 \text{ V}$) ($V_{DD} = \text{max}$, $f = 0 \text{ MHz}$)	I_{SB2}	10	10	mA

NOTE: $\bar{E}1$, $E2$, and $\bar{E}3$ are represented by \bar{E} in this data sheet. $E2$ is of opposite polarity to $\bar{E}1$ and $\bar{E}3$.

CAPACITANCE ($f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25^\circ \text{C}$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance All Inputs Except Clocks and DQs \bar{E} , \bar{G} , \bar{W}	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ±10%, T_A = 0° to 70°C)
 (T_A = -40° to 85°C for Industrial Temperature Option)
 (V_{DD} = 3.3 V +10%, -5% for 10 ns Industrial Device Only)

Input Pulse Levels 0 to 3.0 V	Output Timing Measurement Reference Level 1.5 V
Input Rise/Fall Time 2 ns	Output Load See Figure 1
Input Timing Measurement Reference Level 1.5 V	

READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM6341-10		MCM6341-11		MCM6341-12		MCM6341-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t _{AVAV}	10	—	11	—	12	—	15	—	ns	4
Address Access Time	t _{AVQV}	—	10	—	11	—	12	—	15	ns	
Enable Access Time	t _{ELQV}	—	10	—	11	—	12	—	15	ns	5
Output Enable Access Time	t _{GLQV}	—	4	—	4	—	4	—	4	ns	
Output Hold from Address Change	t _{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t _{ELQX}	3	—	3	—	3	—	3	—	ns	6, 7, 8
Output Enable Low to Output Active	t _{GLQX}	0	—	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High-Z	t _{EHQZ}	0	5	0	6	0	6	0	7	ns	6, 7, 8
Output Enable High to Output High-Z	t _{GHQZ}	0	5	0	6	0	6	0	7	ns	6, 7, 8

NOTES:

1. \bar{W} is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\bar{E}1$, E2, and $\bar{E}3$ are represented by \bar{E} in this data sheet. E2 is of opposite polarity to $\bar{E}1$ and $\bar{E}3$.
4. All read cycle timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with \bar{E} going low.
6. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
7. Transition is measured ±200 mV from steady-state voltage.
8. This parameter is sampled and not 100% tested.
9. Device is continuously selected ($\bar{E} \leq V_{IL}$, $\bar{G} \leq V_{IL}$).

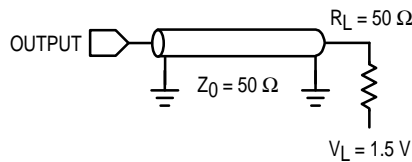
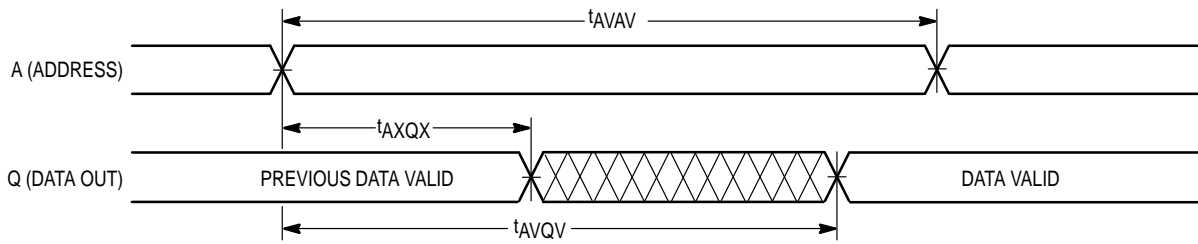
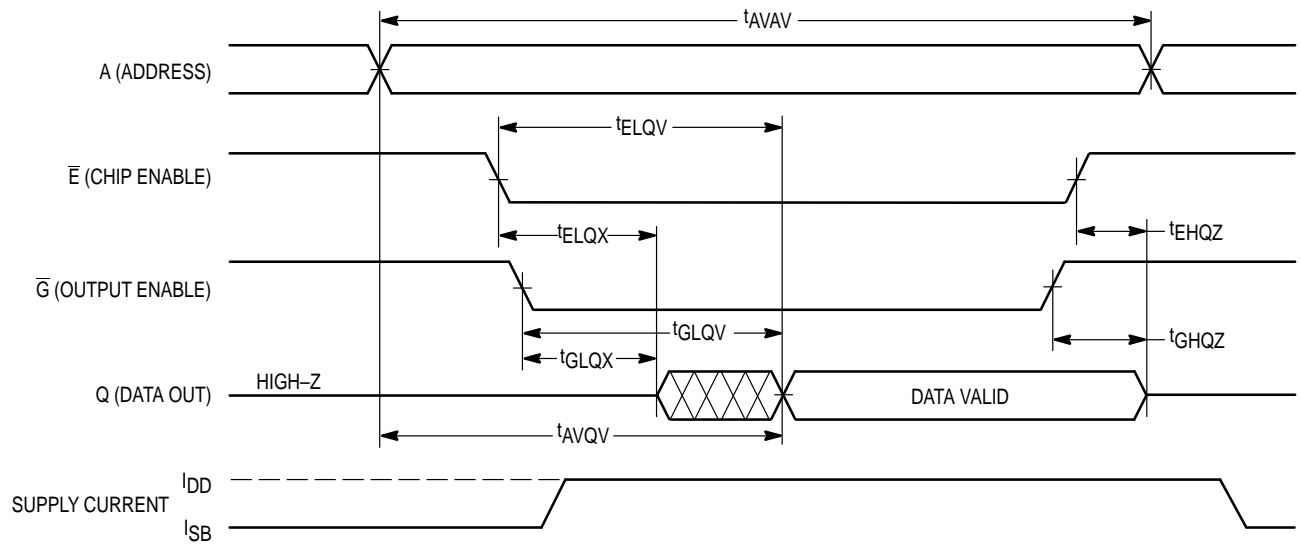


Figure 1. AC Test Load

READ CYCLE 1 (See Note 9)



READ CYCLE 2 (See Notes 3 and 5)

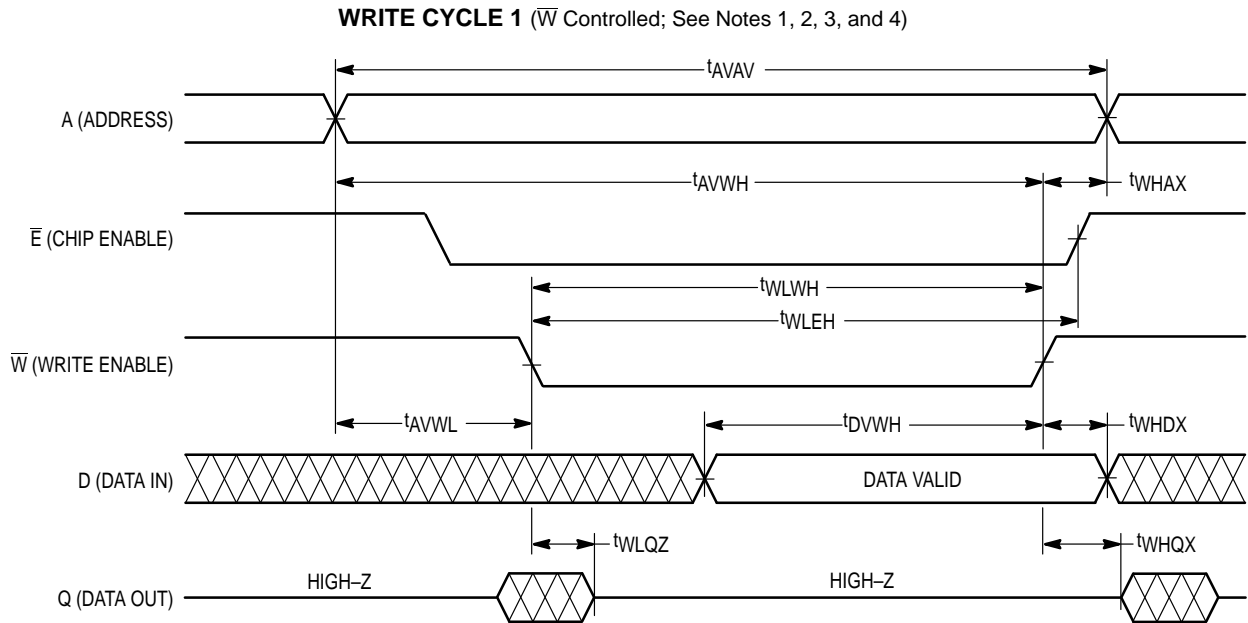


WRITE CYCLE 1 (\overline{W} Controlled; See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM6341-10		MCM6341-11		MCM6341-12		MCM6341-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	11	—	12	—	15	—	ns	5
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	10	—	12	—	ns	
Address Valid to End of Write (\overline{G} High)	t_{AVWH}	8	—	9	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	9	—	10	—	10	—	12	—	ns	
Write Pulse Width (\overline{G} High)	t_{WLWH} t_{WLEH}	8	—	9	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	0	3.5	0	3.5	0	3.5	0	3.5	ns	6, 7, 8
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	6, 7, 8
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If \overline{G} goes low coincident with or after \overline{W} goes low, the output will remain in a high-impedance state.
4. $\overline{E}1$, $\overline{E}2$, and $\overline{E}3$ are represented by \overline{E} in this data sheet. $\overline{E}2$ is of opposite polarity to $\overline{E}1$ and $\overline{E}3$.
5. All write cycle timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured ± 200 mV from steady-state voltage.
7. This parameter is sampled and not 100% tested.
8. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.



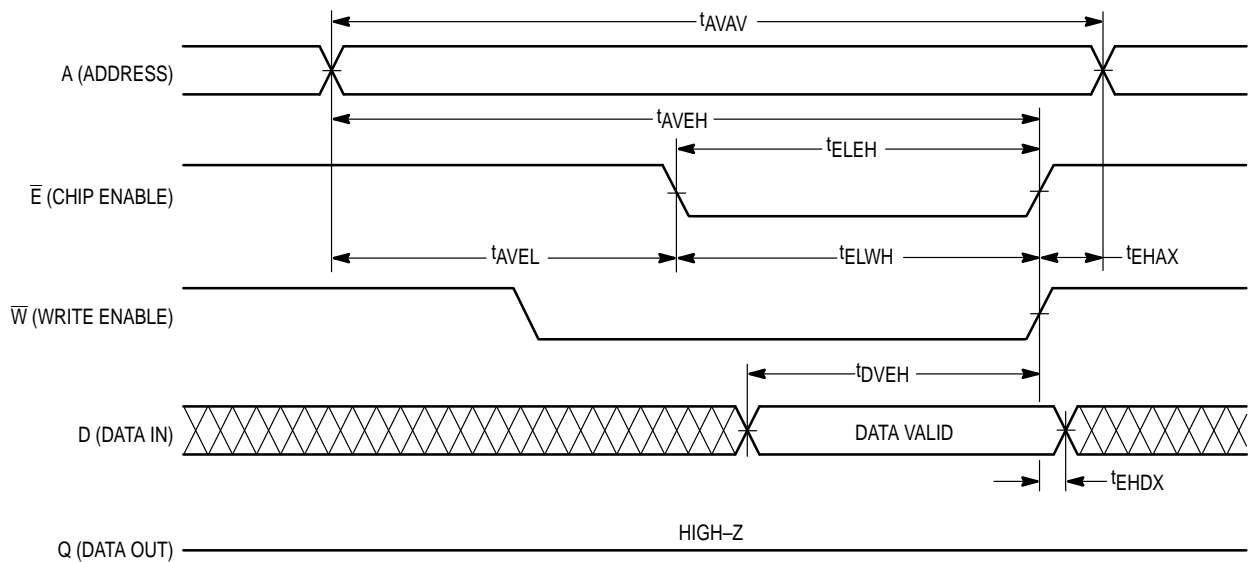
WRITE CYCLE 2 (\bar{E} Controlled; See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM6341-10		MCM6341-11		MCM6341-12		MCM6341-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	11	—	12	—	15	—	ns	5
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	9	—	10	—	10	—	12	—	ns	
Address Valid to End of Write (\bar{G} High)	t_{AVEH}	8	—	9	—	9	—	10	—	ns	
Enable Pulse Width	t_{ELEH} , t_{ELWH}	9	—	10	—	10	—	12	—	ns	6, 7
Enable Pulse Width (\bar{G} High)	t_{ELEH} , t_{ELWH}	8	—	9	—	9	—	10	—	ns	6, 7
Data Valid to End of Write	t_{DVEH}	4	—	5	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:

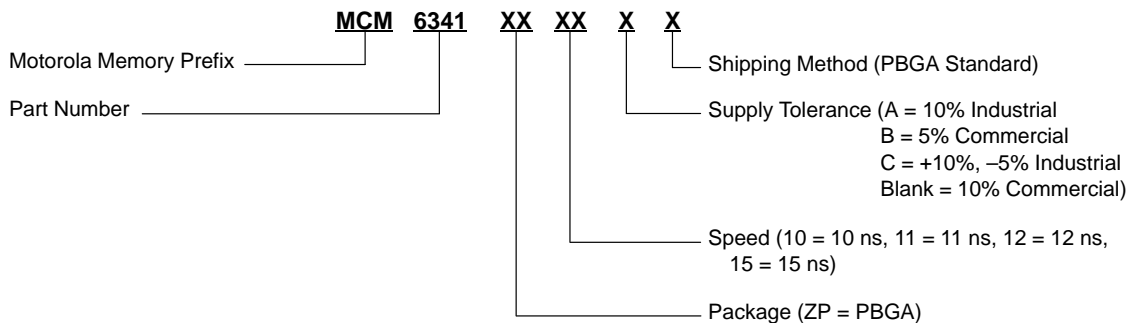
1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If \bar{G} goes low coincident with or after \bar{W} goes low, the output will remain in a high-impedance state.
4. $\bar{E}1$, $E2$, and $E3$ are represented by \bar{E} in this data sheet. $E2$ is of opposite polarity to $E1$ and $E3$.
5. All write cycle timing is referenced from the last valid address to the first transitioning address.
6. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high-impedance condition.
7. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high-impedance condition.

WRITE CYCLE 2 (\bar{E} Controlled; See Notes 1, 2, 3, and 4)



ORDERING INFORMATION

(Order by Full Part Number)

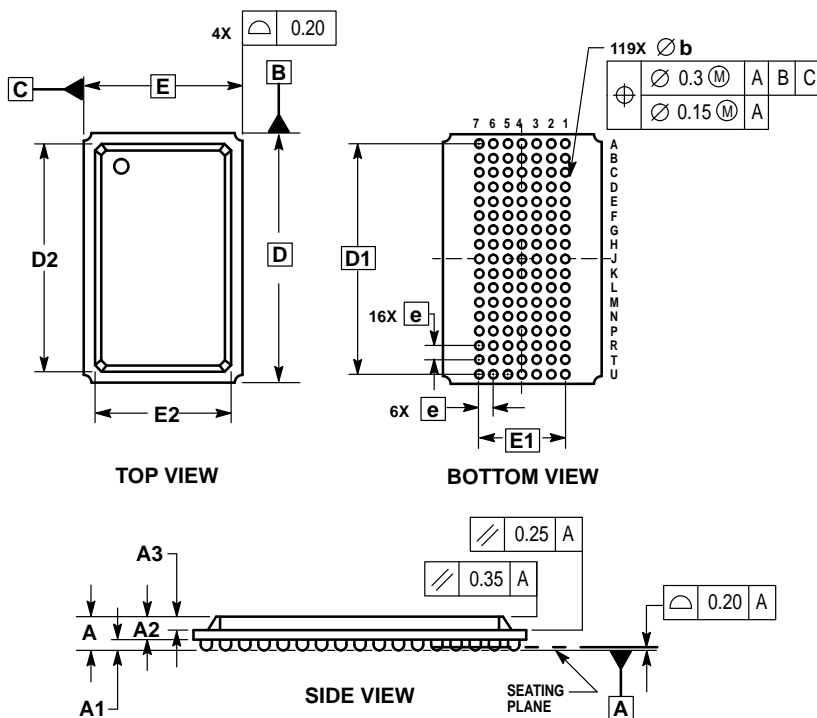


Full Commercial Part Numbers — MCM6341ZP10
 MCM6341ZP11
 MCM6341ZP12
 MCM6341ZP15

Full Industrial Temperature Part Numbers — SCM6341ZP10C
 SCM6341ZP11A
 SCM6341ZP12A
 SCM6341ZP15A


PACKAGE DIMENSIONS

**ZP PACKAGE
 119-PBGA
 CASE 999-02**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. ALL DIMENSIONS IN MILLIMETERS.
 3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
 4. DATUM A, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	—	2.40
A1	0.50	0.70
A2	1.30	1.70
A3	0.80	1.00
D	22.00 BSC	
D1	20.32 BSC	
D2	19.40	19.60
E	14.00 BSC	
E1	7.62 BSC	
E2	11.90	12.10
b	0.60	0.90
e	1.27 BSC	

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